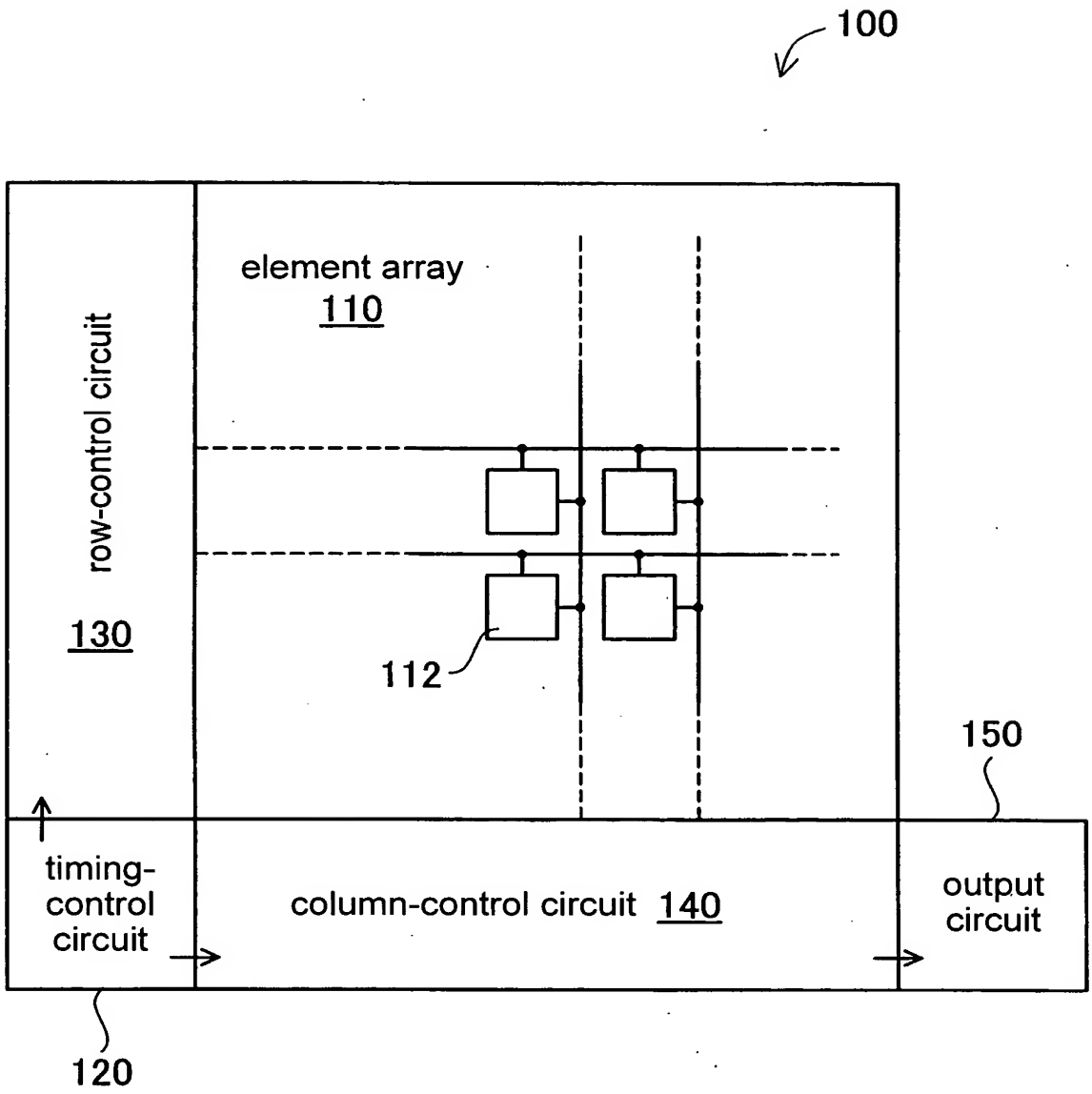
100
element array
110
row-control circuit
130
112
150
timing-
control
circuit
column-control circuit 140
output
circuit
120

FIG. 1

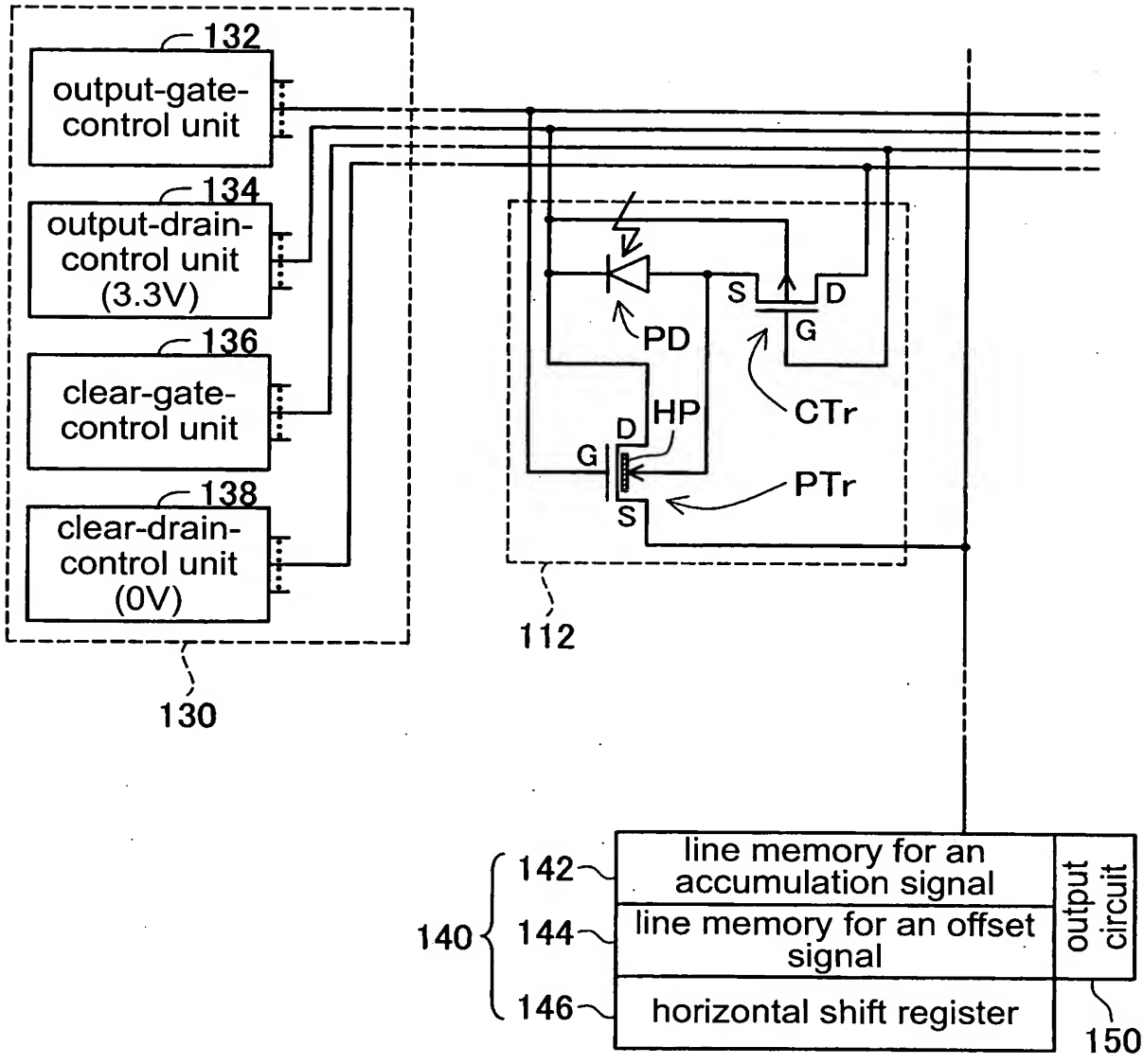
132
output-gate-control unit
134
output-drain-control unit (3.3V)
136
clear-gate-control unit
138
clear-drain-control unit (0V)
130
112
PD
S
D
G
CTr
HP
D
G
PTr
S
140
142
line memory for an accumulation signal
144
line memory for an offset signal
146
horizontal shift register
output circuit
150

FIG. 2

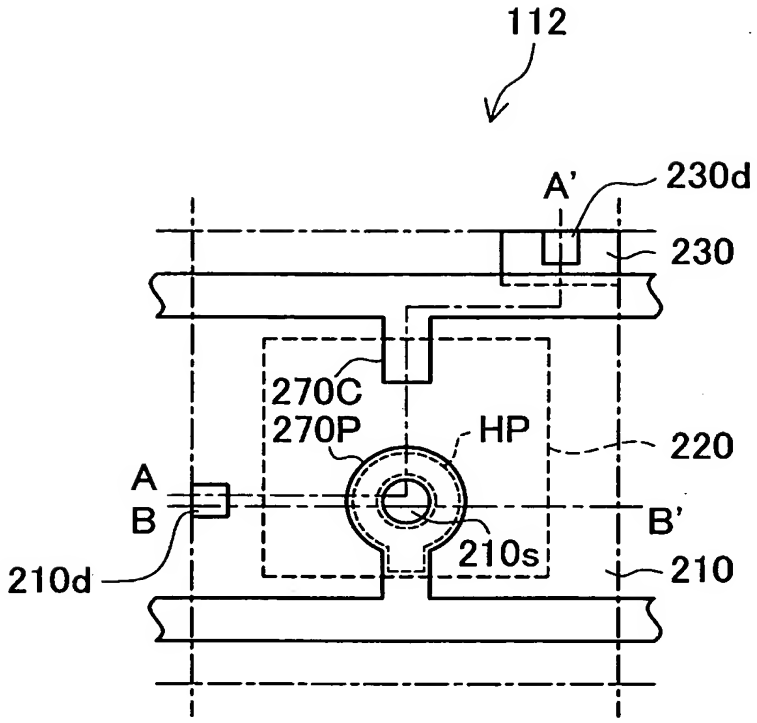
112
A'
230d
230
270C
270P
HP
220
A
B
B'
210s
210d
210

FIG. 3

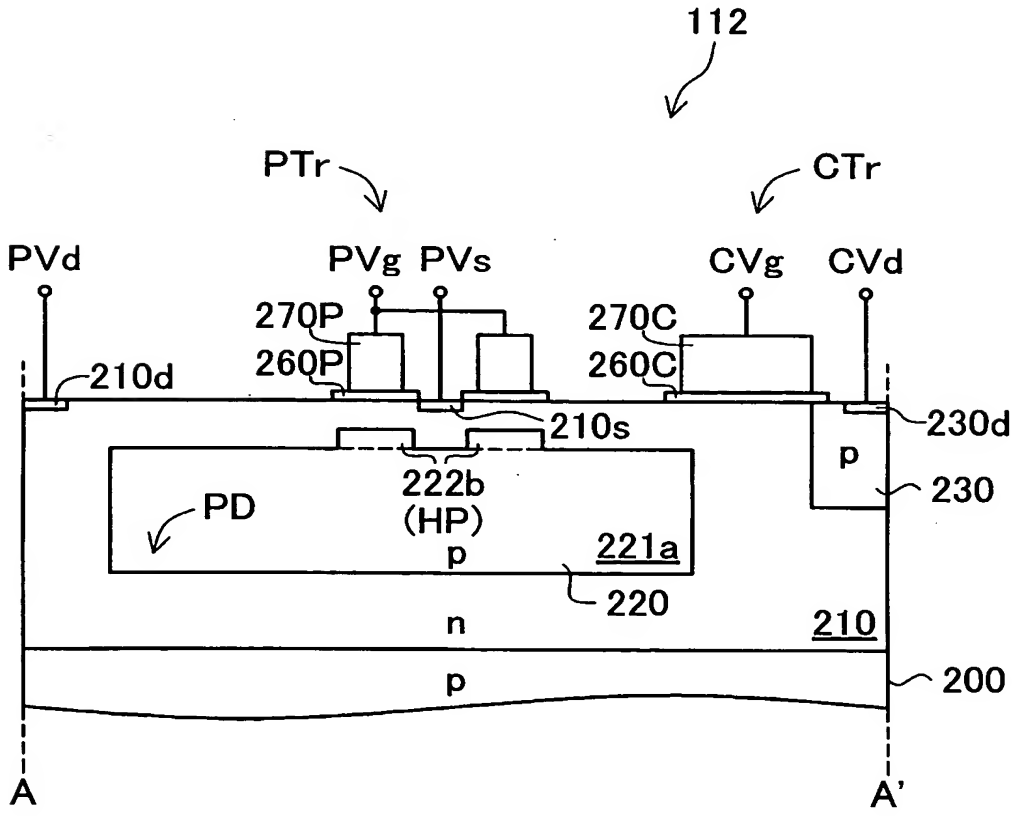
112
PTr
CTr
PVd
PVg
PVs
CVg
CVd
270P
260P
270C
260C
210d
210s
230d
p
230
222b
(HP)
PD
p
221a
220
n
210
p
200
A
A'

FIG. 4

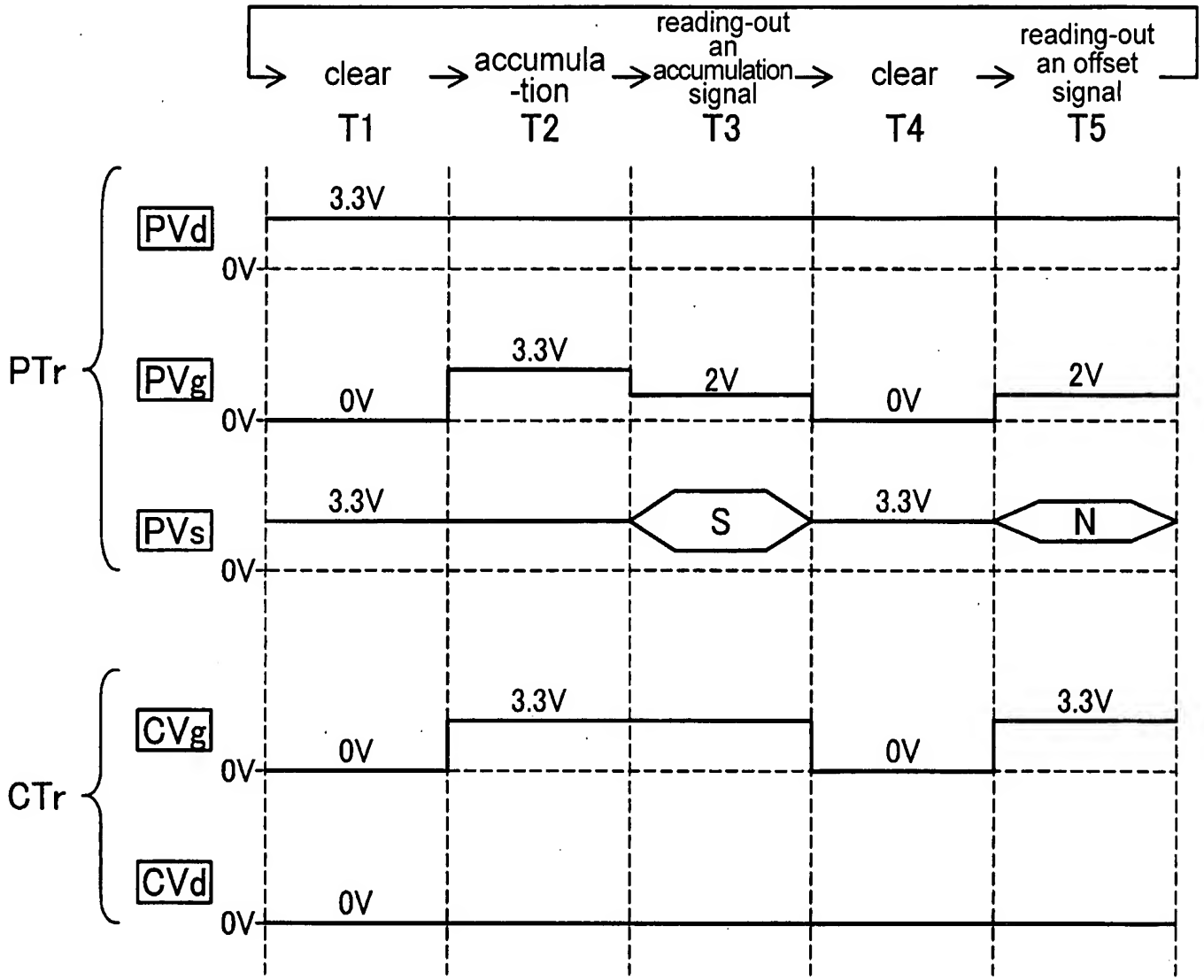
clear
T1
accumula
-tion
T2
reading-out
an
accumulation
signal
T3
clear
T4
reading-out
an offset
signal
T5
PTr
PVd
PVg
PVs
CTr
CVg
CVd
3.3V
0V
2V
S
N

FIG. 5

clear period

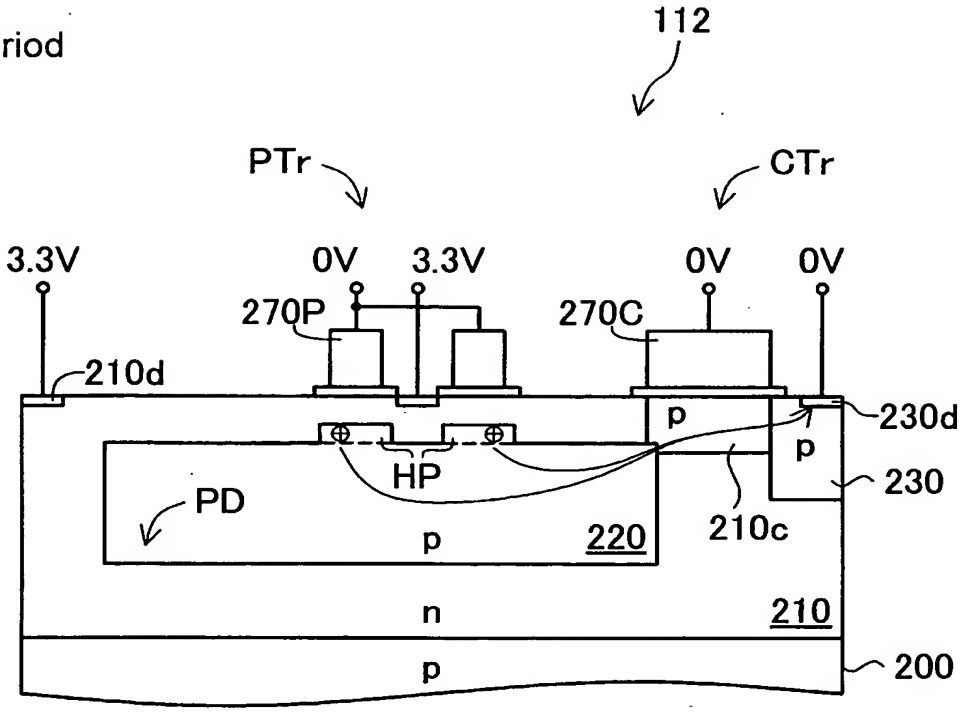


FIG. 6

accumulation period

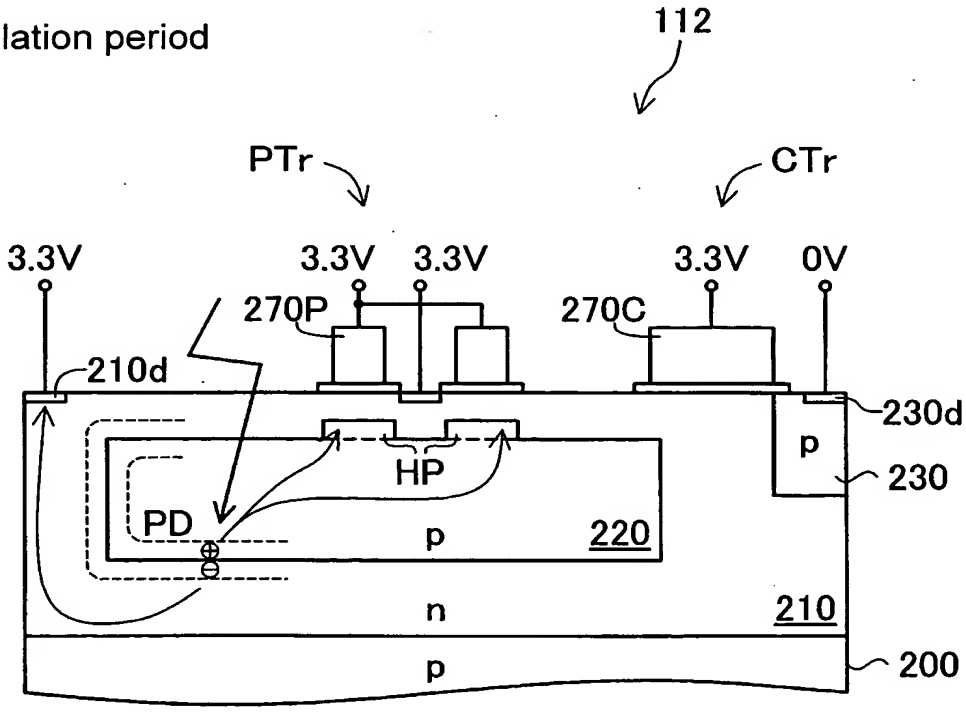


FIG. 7

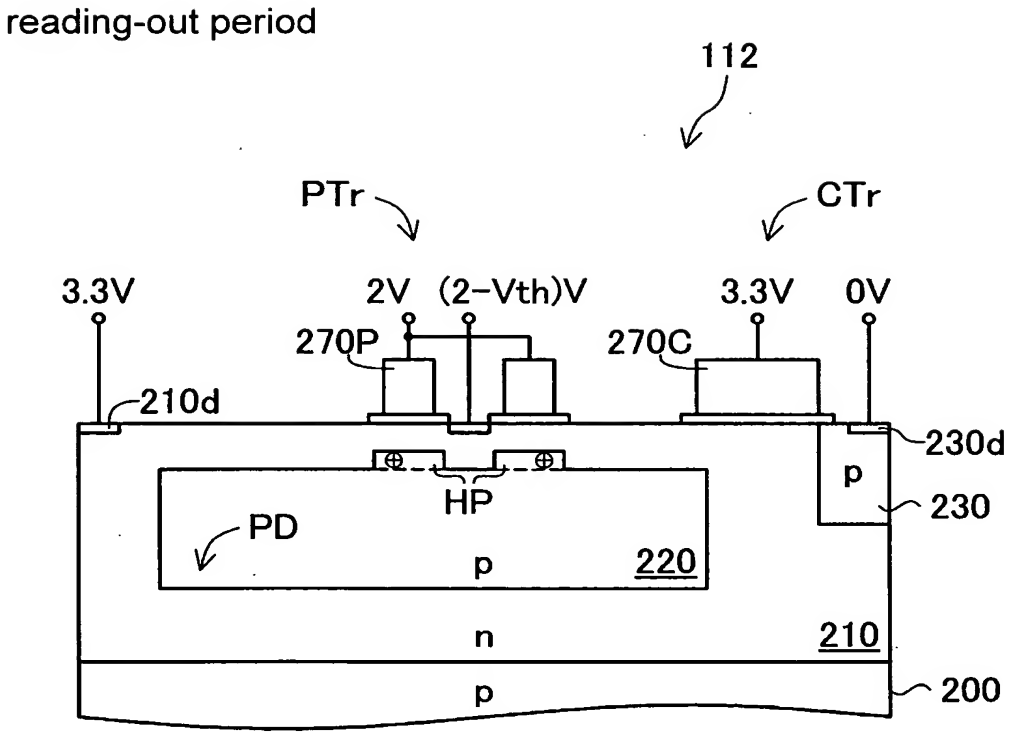
reading-out period
112
PTr
CTr
3.3V
2V
(2−Vth)V
3.3V
0V
270P
270C
210d
230d
p
230
HP
PD
p
220
n
210
p
200

FIG. 8

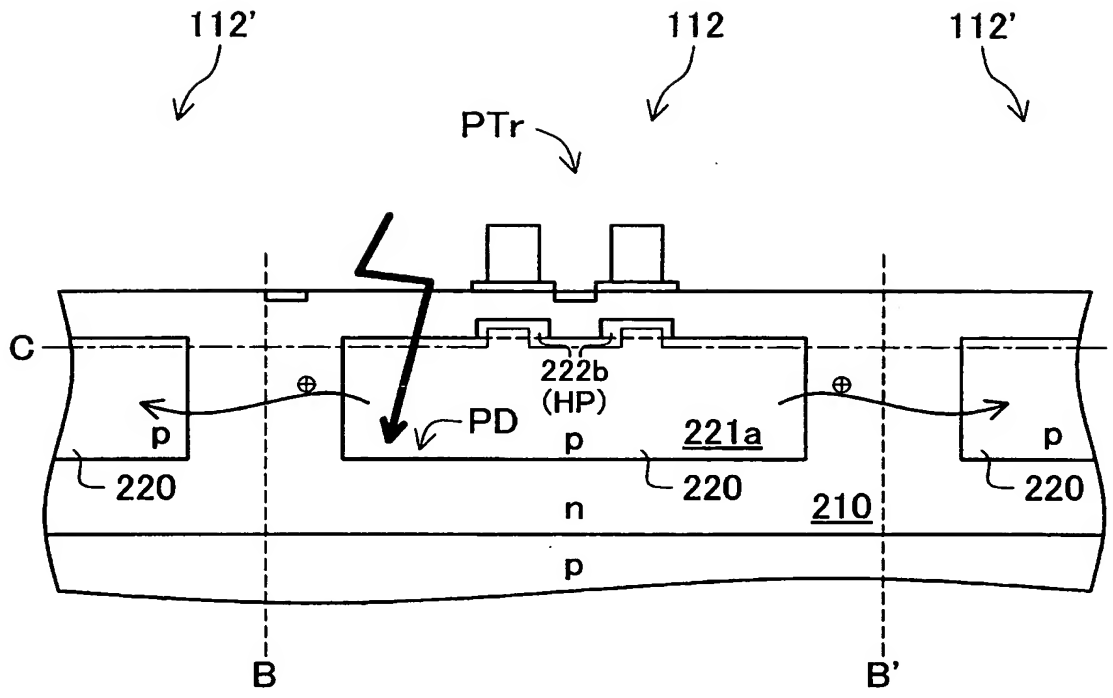
112'
112
112'
PTr
C
222b
(HP)
PD
p
p
221a
p
220
220
220
n
210
p
B
B'

FIG.9A

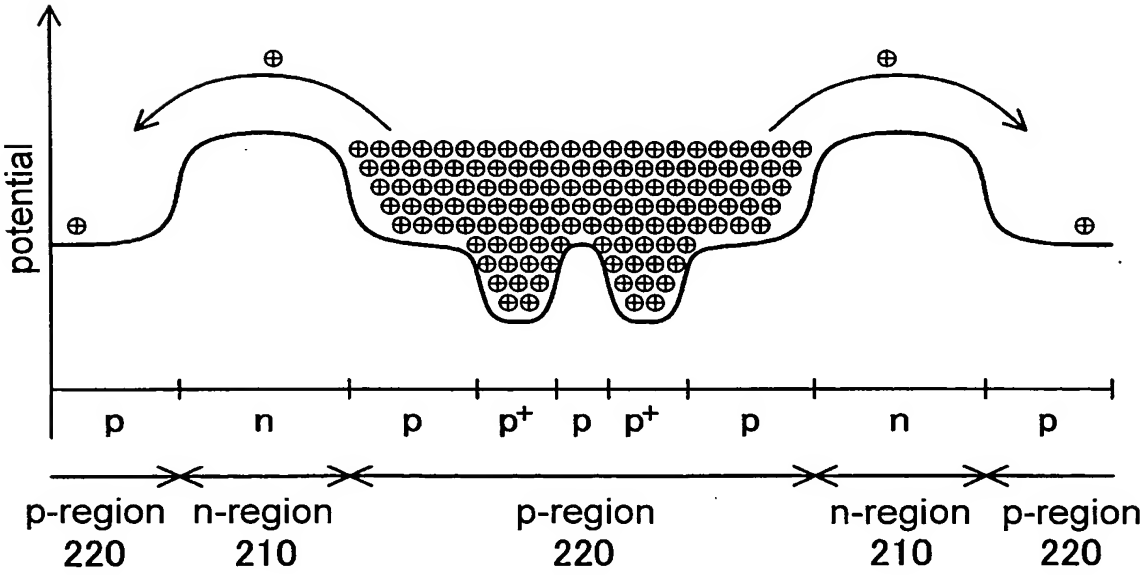
potential
p
n
p
p+
p
p+
p
n
p
p-region
220
n-region
210
p-region
220
n-region
210
p-region
220

FIG.9B

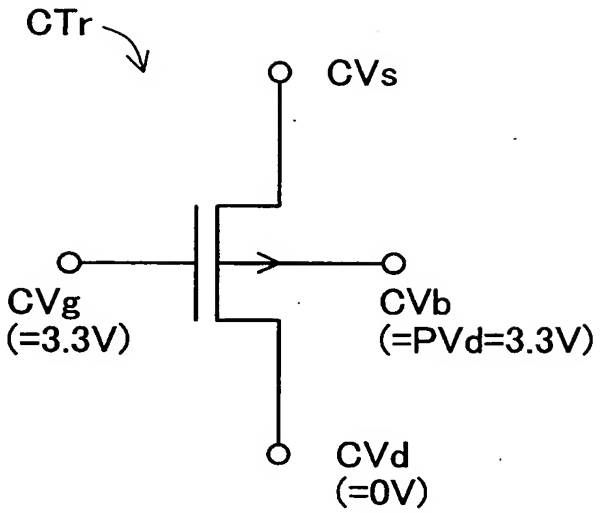
CTr
CVs
CVg
(=3.3V)
CVb
(=PVd=3.3V)
CVd
(=0V)

FIG.10

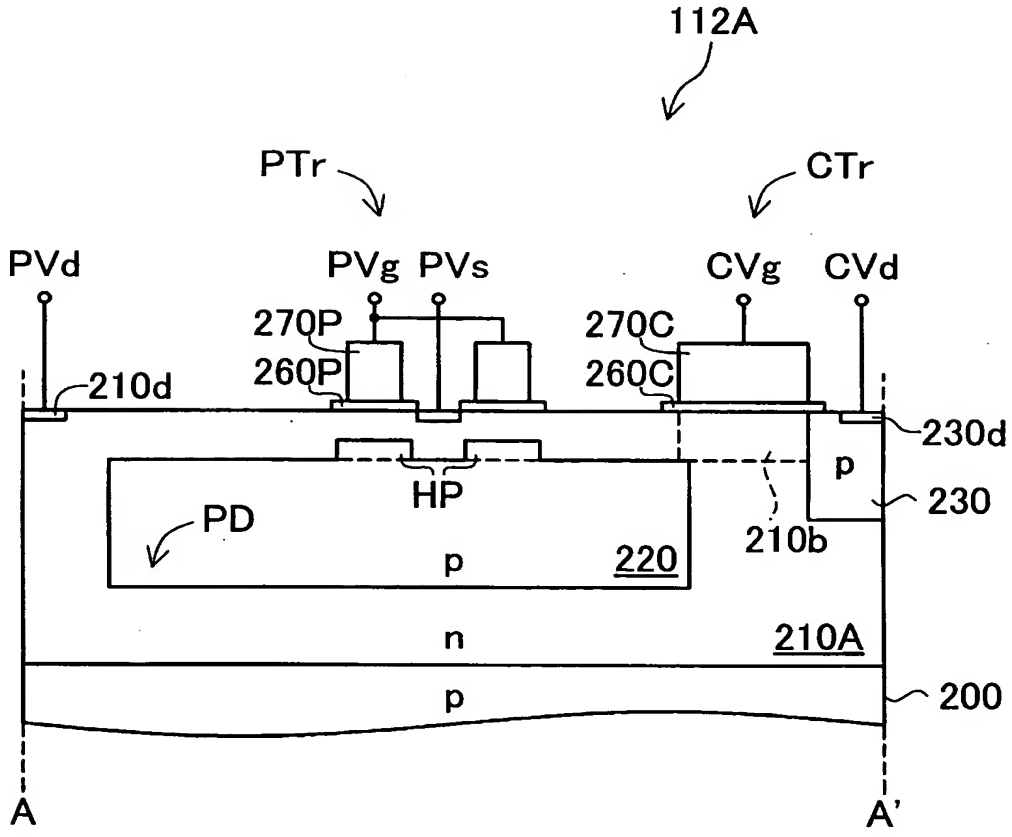
112A
PTr
CTr
PVd
PVg
PVs
CVg
CVd
270P
260P
270C
260C
210d
230d
p
HP
230
PD
210b
p
220
n
210A
p
200
A
A'

FIG.11

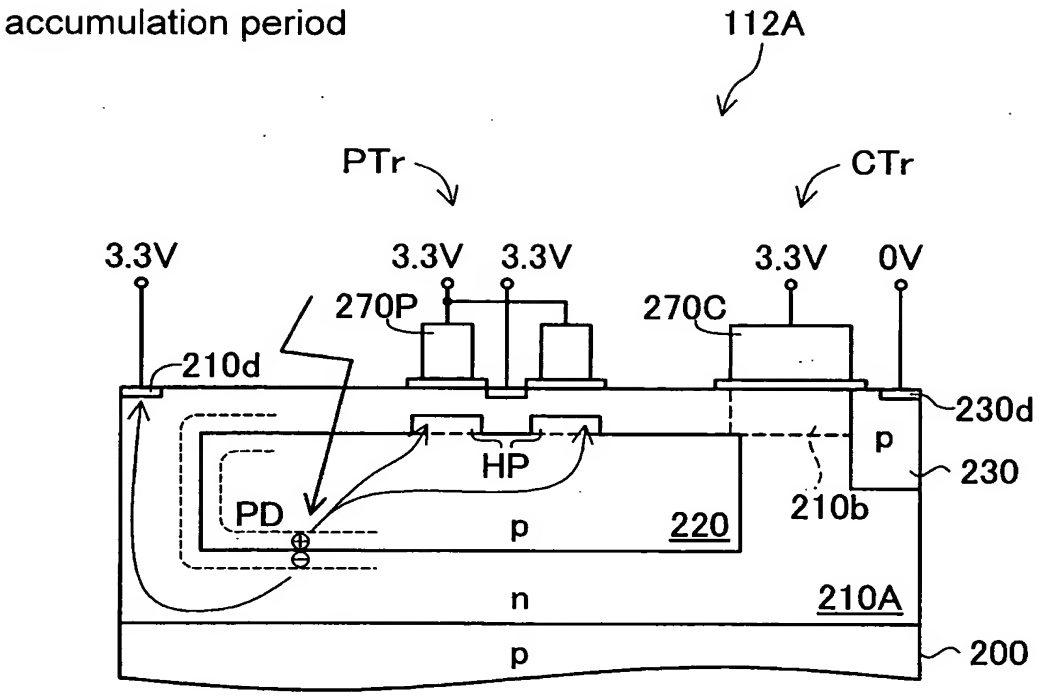


FIG.12A

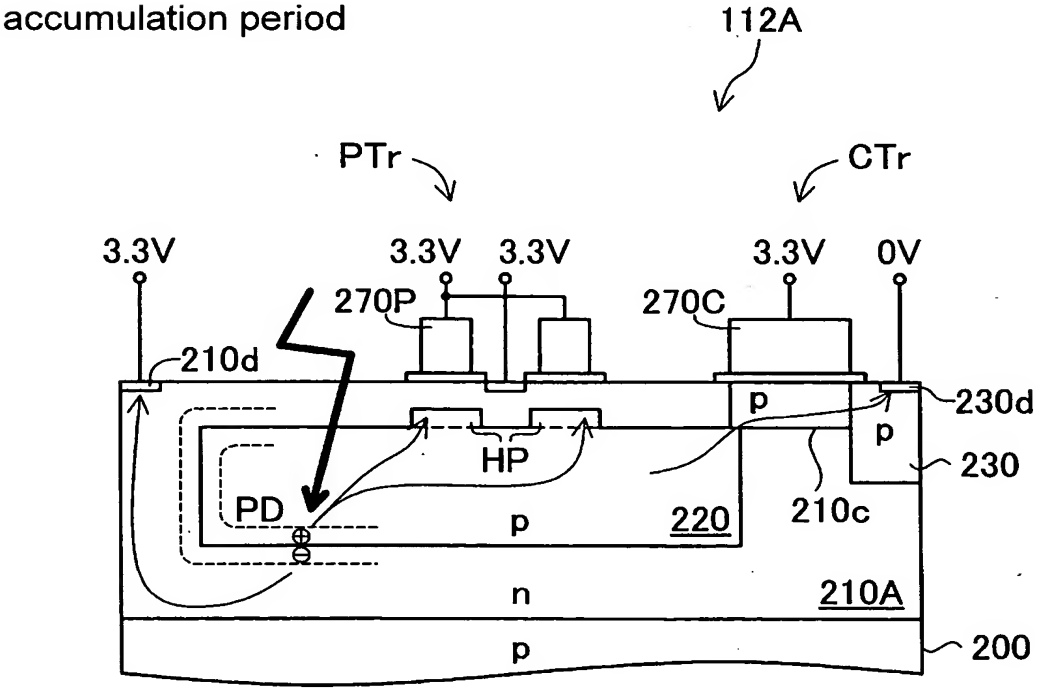


FIG.12B

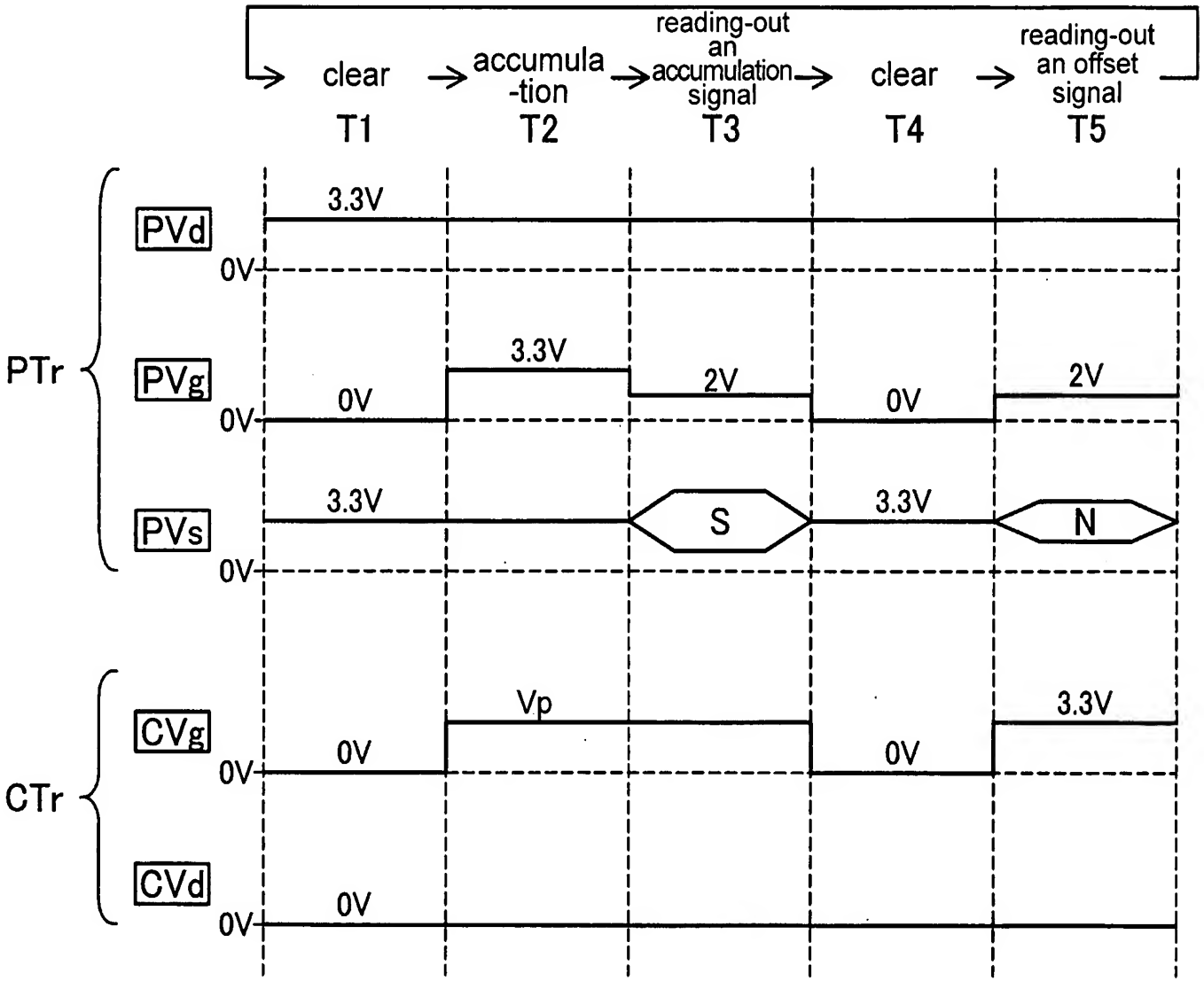
clear
T1
accumula
-tion
T2
reading-out
an
accumulation
signal
T3
clear
T4
reading-out
an offset
signal
T5
PTr
PVd
PVg
PVs
CTr
CVg
CVd
3.3V
0V
2V
S
N
Vp

FIG.13

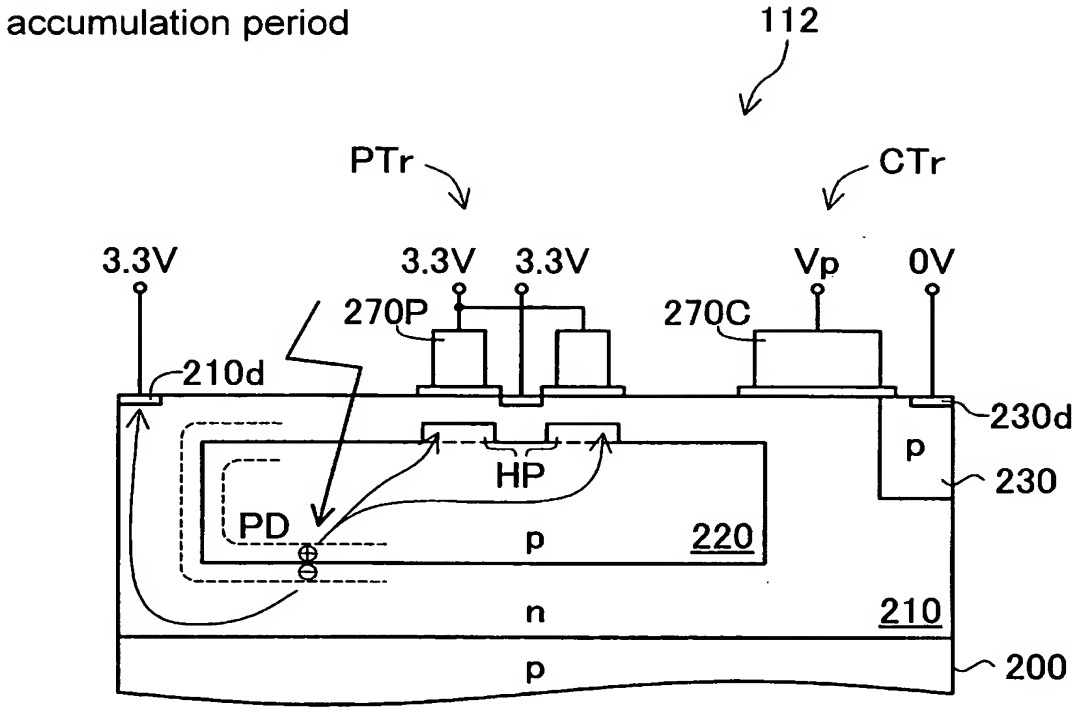


FIG.14A

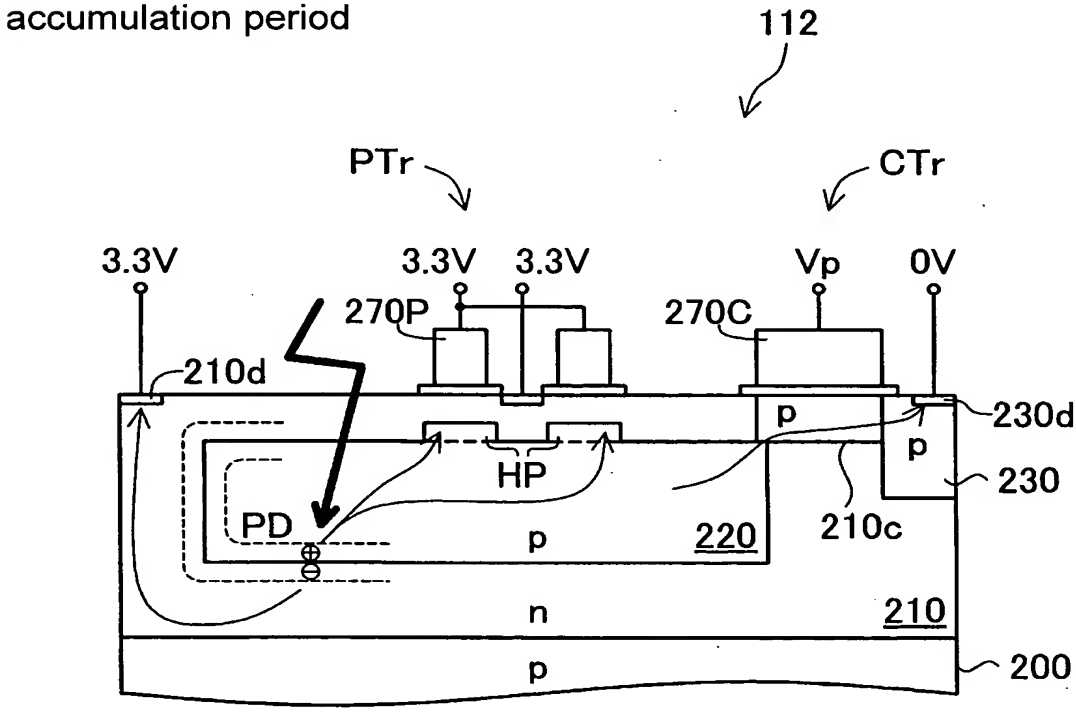


FIG.14B